L3: Entry 27 of 33 File: USPT Aug 18, 1998

DOCUMENT-IDENTIFIER: US 5796391 A
TITLE: Scaleable refresh display controller

Abstract Text (1):
A display controller (112) reduces the power consumed in displaying a graphics image in a portable wireless communications device (100) when a graphics image is smaller than the size of the display (118). The number of rows and columns used to display the graphics image is counted by a decoder (108) which is a microcontroller used to operate the communications device (100). The decoder (108) provides the reduced row or column count to the display controller (112), which reduces the frequencies of clocks (PIXEL CLOCK, LINE PULSE, FRAME PULSE) used for timing data transfers to the display (118). Power is reduced by operating the display (118) at a lower frequency while acceptable frame refresh rates are maintained.

Parent Case Text (2):
The present application is related to copending U.S. patent application, Attorney's Docket No. SC09887C, entitled "DISPLAY DRIVER AND METHOD THEREOF," filed Oct. 24, 1996, U.S. patent Ser. No. 08/740,052, by Inventors Scott Chiu and Scott Novis; and patent application, Attorney's Docket No. SC09960C, entitled "NONLINEAR GRAY SCALE METHOD AND APPARATUS," filed Oct. 24, 1996, U.S. patent Ser. No. 08/740,055, by Inventors Scott Chiu, Karen Jachimowicz and George Kelly; and assigned to the same assignee, Motorola Inc.

Brief Summary Text (2):
The present application is related to copending U.S. patent application, Attorney's Docket No. SC09887C, entitled "DISPLAY DRIVER AND METHOD THEREOF," filed Oct. 24, 1996, U.S. patent Ser. No. 08/740,052, by Inventors Scott Chiu and Scott Novis; and patent application, Attorney's Docket No. SC09960C, entitled "NONLINEAR GRAY SCALE METHOD AND APPARATUS," filed Oct. 24, 1996, U.S. patent Ser. No. 08/740,055, by Inventors Scott Chiu, Karen Jachimowicz and George Kelly; and assigned to the same assignee, Motorola Inc.

Brief Summary Text (4):
The present invention relates in general to display control circuits and more particularly to display control circuits in which the display is scaled down to fit an image.

Brief Summary Text (5):
Wireless communications devices typically receive a transmitted signal which contains information communicated to a user on a display. For example, a pager receives a transmitted signal modulated with digital data in a predefined format. A decoder in the pager is preprogrammed to recognize the predefined format and to perform computations on the digital data for recovering display and control data for operating the display.

Brief Summary Text (6):
The increasing functionality of pagers requires a graphics user interface (GUI) to make pagers easier to program and operate. A GUI includes a display controller which drives a high resolution light-emitting device (LED) display for viewing graphics images such as status icons and downloaded facsimile messages. A typical

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LED display is organized into a plurality of rows and columns. An image is displayed by scanning columns and activating rows to illuminate the pixels in the column.

Brief Summary Text (7):
Displaying graphics images requires the display controller to process and transfer large amounts of display and control data. A high frequency clock is needed for transferring data and for maintaining acceptable frame refresh rates for flicker-free display operation. However, high frequencies generate radio frequency interference and increase power consumption in the display and the display controller. The radio frequency interference lowers the performance of a portable wireless communications device while higher power consumption reduces the operating time between battery charges.

Brief Summary Text (8):
Hence a high resolution display controller is needed whose power consumption can be reduced while maintaining flicker-free frame refresh rates.

Drawing Description Text (3):
FIG. 2 is a block diagram of a display controller; and

Drawing Description Text (4):
FIG. 3 shows a display with associated row and column drive circuitry.

Detailed Description Text (2):
FIG. 1 shows a block diagram of a portable wireless communications device 100, such as a pager or cellular telephone. Antenna 102 receives a transmitted radio frequency (RF) carrier signal modulated with digital data in a predefined format, including control data for operating communications device 100 and display data for viewing text and/or graphics images on a display 118. The RF carrier signal is coupled to RF receiver 104 for tuning and amplification. A demodulator 106 receives the amplified RF carrier signal and recovers a baseband digital data stream at its output.

Detailed Description Text (3):
Decoder 108 comprises a microcontroller which is preprogrammed to receive the baseband digital signal and to apply the predefined format to recover video and control components. The video component includes display data comprising a series of eight-bit luminance bytes. Each byte includes two four-bit luminance words which provide information for illuminating two pixels in display 118. The luminance bytes are provided on an eight-conductor bus 120 coupled to a graphics display random access memory (RAM) 110, a row driver 116 and a display controller 112. Although bus 120 is shown as an eight-conductor bus, it should be apparent that data can be provided on a wider or narrower bus as appropriate in a particular embodiment.

Detailed Description Text (4):
The control component includes end-of-line and end-of-frame synchronization signals for reproducing the image on display 118. As the baseband digital signal is processed, decoder 108 counts pixels until an end-of-line synchronization signal is received, thereby computing a pixel count, which represents the number of pixels in a line of the image. Decoder 108 counts lines of the image until an end-of frame signal is received for computing a line count which represents the number of lines in an image frame. The pixel count and line count are provided to display controller 112 on bus 120 accompanied by associated control signals provided on a two-conductor control bus 122. Decoder 108 divides the maximum number of pixels in a line, e.g., 72 pixels per line, by the pixel count to produce a pixel-rate divisor for adjusting the frequency of a PIXEL CLOCK used for timing data transfers on bus 120. Decoder 108 is also programmed to track where image data is stored in graphics display RAM 110 to provide efficient memory utilization.

Detailed Description Text (5):
Decoder 108 performs tasks in communications device 100 not related to displaying images, such as processing downloaded data and interpreting keypad commands. Many display functions are managed by display controller 112, while other control functions are provided by decoder 108. For example, display controller 112 provides incremental memory addresses to graphics display RAM 110 for storing or retrieving downloaded images, but the starting address is provided by decoder 108. A key function of display controller 112 is to minimize power consumption by dynamically adjusting the frequency of data transfers to operate display 118 at the lowest frequency which both reproduces the displayed image and refreshes display 118 at a flicker-free rate. Timing for display controller 112 is provided by a system clock V.sub.SYSTEM operating at a rate of 2.5 megahertz.

Detailed Description Text (6):
Display controller 112 generates a LINE PULSE and a FRAME PULSE on a two-conductor bus 124 which are coupled to column driver 114 for respectively scanning columns and refreshing display 118. A PIXEL CLOCK is produced on bus 126 for clocking display data to row driver 116. A LINE PULSE is generated at bus 126 for resetting row driver 116 to load display data in the first row of display 118.

Detailed Description Text (7):
Graphics display RAM 110 includes an array of read-write storage cells operating as a buffer for storing downloaded display data. Internal images such as status icons which are typically stored in read-only memory (not shown) are also transferred to graphics display RAM 110 for easier accessibility. The timing of transfers of display data to and from graphics display RAM 110 is managed by display controller 112.

Detailed Description Text (8):
Display 118 comprises a matrix of light-emitting devices (LED) such as light-emitting diodes organized into a plurality of rows and columns to operate as pixels of display 118. In one embodiment of communications device 100, display 118 has 72 rows and 120 columns. The cathodes and anodes of the LED pixels are respectively connected to rows and columns in display 118 such that a unique LED pixel is illuminated when a column is selected and a row is activated. Rows and columns are respectively coupled to row and column inputs of display 118.

Detailed Description Text (9):
Column driver 114 has a plurality of outputs coupled to the column inputs of display 118 to operate in a column scan mode in which one column at a time is selected. Successive columns are selected by repetitively clocking column driver 114 with a LIME PULSE. When column driver 114 scans to the last display column of an image, a FRAME PULSE resets column driver 114 to cycle back to the first display column for refreshing display 118.

Detailed Description Text (10):
Row driver 116 has a plurality of outputs which operate in parallel to provide activating pulses to row inputs of display 118 for illuminating LED pixels in the selected column. The activating pulses drive LED pixels to a luminance level determined by four-bit luminance words. Pairs of luminance words are combined into an eight-bit luminance byte and serially clocked into respective pairs of individual cells of row driver 116 by PIXEL CLOCK. When all of the luminance words in a display column have been loaded, display controller 112 issues a LINE PULSE to cycle row driver 116 back to the first pair of cells to load new data.

Detailed Description Text (11):
FIG. 2 shows a block diagram of display controller 112 which is a clocking circuit including latches 202, 208, 212 and 216; programmable dividers 204,210 and 214; an address decoder 206 and an address counter 218. Display controller 112 sets the timing of data transfers among decoder 108, graphics display RAM 110 and row driver

116 in accordance with the size of the displayed image. Timing is varied by dynamically adjusting the frequency of PIXEL CLOCK and the periods of LINE PULSE and FRAME PULSE.

Detailed Description Text (16):
Programmable divider 210 comprises a free-running, four-bit parallel-load down counter. The pixel count is loaded from bus 120 into latch 208 in response to a load signal from address decoder 206, and coupled to a four-bit parallel input of programmable divider 210. Because two luminance words at a time are clocked into row driver 116, the value of the pixel count represents one-half the number of pixels of display data within a column. The pixel count thus ranges in value from 4 to 36. Programmable divider 210 decrements on pulses of PIXEL CLOCK and produces a LINE PULSE upon reaching a zero count. After a LINE PULSE is produced, programmable divider 210 resets to the pixel count and begins the next cycle.

Detailed Description Text (17):
Latch 212 comprises a four-bit parallel-load, parallel output latch which operates in conjunction with programmable divider 214 to control when a FRAME PULSE is generated. A FRAME PULSE resets column driver 114 to select the first column for refreshing display 118. The line count is loaded from bus 120 into latch 212 in response to a load signal from address decoder 206, and coupled to a four-bit parallel input of programmable divider 214. A FRAME PULSE is generated after column driver 114 has successively scanned all of the columns in the displayed image.

Detailed Description Text (19):
Most if not all logic families increase power consumption when the operating frequency increases. The power is typically consumed during logic level transitions when logic gates charge and discharge parasitic capacitances. Additional power is consumed by current spikes which are generated because of delays in turning off transistors in logic gates. When power is consumed at higher frequencies, more RF interference is generated. Besides system clock V.sub.SYSCLK, PIXEL CLOCK operates at the highest dock frequency in communications device 100. Accordingly, PIXEL CLOCK is a source of substantial power consumption when operating at the 1.25 MHz frequency needed for driving display 118 in a full display mode. Smaller images, such as telephone numbers or status icons are fully displayed in fewer rows and columns of display 118 and require fewer data transfers between frame refreshes. If these smaller images are displayed using the maximum 1.25 MHz frequency of PIXEL CLOCK, power is unnecessarily wasted.

Detailed Description Text (20):
The present invention reduces overall power consumption by determining the size of an image and dynamically adjusting clock operating frequencies to transfer data at the lowest frequency that ensures an acceptable refresh rate. For a LED display or other zero persistence display, the minimum refresh rate for flicker-free operation has been determined to be 52.8 hertz. The frequency of PIXEL CLOCK and LINE PULSE are reduced when an image can be displayed with fewer pixels per line, i.e., on fewer rows. The frequency of FRAME PULSE is reduced when the image is displayed using fewer columns. By way of example, for a minimum image size having a square whose dimension is eight pixels on a side, the frequency of PIXEL CLOCK is reduced to approximately (1.25 MHz)/9=137 kilohertz.

Detailed Description Text (21):
Latch 216 comprises an eight-bit parallel-load, parallel output latch which operates in conjunction with address counter 218 to provide addresses to graphics display RAM 110 for storing luminance bytes. The starting address for the first luminance byte is provided by decoder 108 to provide ready access to recently displayed images in order to minimize power consuming data transfers. The starting address is loaded from bus 120 into latch 216 and coupled to address counter 218 by a load pulse from address decoder 206. Successive luminance bytes are stored at incremental addresses generated by address counter 218 in response to PIXEL CLOCK.

Address counter 218 is an eight-bit, parallel-load up counter which has a capacity to generate 256 unique addresses. For images requiring more address space, luminance data can be stored in 256-address pages, where a page address is produced in decoder 108 and coupled on bus 120 directly to graphics display RAM 110.

Detailed Description Text (22):
Referring to FIG. 3, a diagram of display 118 is shown being driven by row and column drivers 116 and 114, respectively. Display 118 comprises a LED matrix coupled to 72 rows and 120 columns to operate each LED as a display pixel. A LED pixel is illuminated when its associated column is selected and its row is driven by an activating signal.

Detailed Description Text (23):
Column driver 114 includes a 120-stage shift register 308 having a feedback output at the last stage coupled to the data input of the first stage to operate shift register 308 as a ring counter. The FRAME PULSE is applied at an input for initializing shift register 308 to produce a column enable signal at the output of the first stage for selecting the first column. The LINE PULSE repetitively applied to the clock input of shift register 308 clocks the column enable signal through successive stages to operate display 118 in a column scan mode.

Detailed Description Text (24):
When display 118 is operating such that all 120 columns are used for displaying an image, shift register 308 operates as a ring counter which shifts the column select signal from the last stage (stage 119) back to the first stage (stage 0) through the feedback output. When the image is displayed on fewer than 120 columns, the FRAME PULSE is produced after the last column has been selected, thereby reinitializing shift register 308 and selecting the first column. For example, if columns 0 through 19 are used for displaying an image, shift register 308 repetitively selects columns 0 through 19. On the next clock cycle, the FRAME PULSE is applied by display controller 112, which initializes shift register 308 and selects column 0 again. Instead of scanning all 120 columns, column driver 114 scans only columns 0-19 needed for displaying the image. The frequencies of the LINE PULSE and FRAME PULSE are therefore reduced accordingly. In an alternative embodiment, shift register 308 includes parallel inputs which load data representative of a starting column in response to the FRAME PULSE to display an image at any column of display 118.

Detailed Description Text (27):
Row driver cell 304 has an output coupled to a row input of display 118. The output provides an activating signal for illuminating a LED pixel in the selected column. Row driver cell 304 comprises a flip-flop which is clocked by the LINE PULSE to load a luminance bit and initiate the activating signal as determined by the value of the luminance bit. Alternatively, gray scale pixel shading is provided by a digital-to-analog converter (not shown) whose output provides the activating signal having an amplitude determined by the value of the luminance word. The amplitude of the activating signal defines a current in the LED pixel for producing a variable luminance.

Detailed Description Text (30):
In full display mode, 36 pulses of PIXEL CLOCK increment row address counter 302 to count row addresses from 0-35. Where the image size is reduced, a LINE PULSE reinitializes row address counter 302 to a zero count after loading a luminance word into the last row of the displayed image. For example, if an image is displayed using 40 rows, i.e., 20 row addresses, then row address counter 302 counts from 0-19 and a LINE PULSE reinitializes row address counter 302 back to a 0 count.

Detailed Description Text (31):
The present invention thereby provides a display controller for displaying a

graphics image in a portable wireless communications device which operates at a reduced power level. The number of rows and columns in the displayed graphics image is counted by a decoder, which provides line and frame counts to the display controller for adjusting the period of a LINE PULSE and a FRAME PULSE to correspond to the image size. The decoder produces a pixel-rate divisor which is loaded into a binary counter in the display controller to reduce the frequency of the PIXEL CLOCK when fewer data transfers are needed to display the image.

Detailed Description Text (32):
By continuously monitoring the number of rows and columns in the displayed image, the present invention is able to dynamically adjust the PIXEL CLOCK, LINE PULSE and FRAME PULSE frequencies to the lowest value which allows the image to be displayed without display flicker. The reduced frequency operation reduces the power consumed by column driver 114 and row driver 116 during logic level transitions resulting from current spikes in the logic gates and the charging and discharging of parasitic voltages. Besides extending battery operating time, the reduced frequencies improve the performance of the portable wireless communications device by reducing RF interference.

CLAIMS:

1. A wireless communications device for viewing an image on a display, comprising:

a radio frequency (RF) circuit having an input coupled for receiving a RF input signal and an output;

a demodulator having an input coupled to the output of the RF circuit and having an output for providing a baseband data signal;

a decoder circuit having an input for receiving the baseband data signal for providing image data, where the decoder circuit counts a number of pixels within a line of the image data to produce a pixel count and divides a number of pixels within a line of the display by the pixel count to compute a pixel rate divisor;

a circuit for clocking the display, including

(1) a first divider having a clock input for receiving a clock signal, a data input for receiving the pixel rate divisor, and an output for providing a pixel clock for transferring the image data to the display; and

(2) a second divider having a clock input for receiving the pixel clock, a data input for receiving the pixel count, and an output for providing a line clock having a substantially constant period as a period of the pixel clock varies.

2. A clocking circuit for driving a display device, comprising:

a decoder circuit having an input for receiving a data stream and an output for providing image data, the decoder circuit counting a number of pixels within a line of the image data to produce a pixel count and dividing a number of pixels within a line of the display device by the pixel count to compute a pixel rate divisor;

a first divider having a clock input for receiving a clock signal, a data input for receiving the pixel rate divisor, and an output for providing a pixel clock for transferring the image data; and

a second divider having a clock input for receiving the pixel clock, a data input for receiving the pixel count, and an output for providing a line clock having a substantially constant period as a period of the pixel clock varies.

10. A method of clocking a display, comprising the steps of:

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counting a number of pixels within a line of the image data to produce a pixel count;

dividing a number of pixels within a line of the display by the pixel count to compute a pixel rate divisor;

counting a system clock to the pixel rate divisor to produce a pixel clock for transferring the image data; and

counting the pixel clock to the pixel count to produce a line clock having a substantially constant period as a period of the pixel clock varies.

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DOCUMENT-IDENTIFIER: US 5619707 A
TITLE: Video subsystem power management apparatus and method

Abstract Text (1):
Power is conserved in a video subsystem by inactivating a pixel clock (PCLK) and reducing frequency of a memory clock (MCLK) responsive to an indication of user inactivity. The inactivation of PCLK reduces the power consumed in the RAMDAC, frame buffer, phase lock loop (PLL) clock circuit, and to a smaller extent, the video controller. Reducing the frequency of MCLK conserves power in the video controller and the PLL, while maintaining the integrity of the data in the frame buffer. Significant power savings can be accomplished with minimal BIOS or video controller programming and minimal transfer of state information prior to power-down.

Brief Summary Text (11):
The present invention reduces power in a video subsystem by generating signals to a display of a computer system to reduce power to the display, inactivating a pixel clock which coupled to a RAMDAC and decreasing the frequency of a memory clock for driving a video controller by a predetermined factor, thereby reducing the power consumed by the video controller.

Brief Summary Text (12):
The present invention provides significant advantages over the prior art. The inactivation of PCLK reduces the power consumed in the RAMDAC, frame buffer, phase lock loop (PLL) clock circuit, and to a smaller extent, the video controller. Reducing the frequency of MCLK conserves power in the video controller and the PLL, while maintaining the integrity of the data in the frame buffer. Significant power savings can be accomplished with minimal BIOS or video controller programming and minimal transfer of state information prior to power-down.

Detailed Description Text (2):
FIG. 1 illustrates a block diagram of a general computer system 10. The computer system 10 comprises a CPU motherboard 12 coupled to a video subsystem 14, hard disk 16 and other peripherals, generally referenced at numeral 18, over bus 20. The video subsystem 14 is coupled to display 22. It should be noted that the block diagram of FIG. 1 presents a general architecture for a computer system. Many features formally coupled to the bus 20 have been incorporated into the system motherboard in present-day designs. The present invention, which concerns power management of the video subsystem 14, is effective for both video cards for connection to a bus and integrated video circuitry on the motherboard.

Detailed Description Text (3):
In personal computers which operate under the MICROSOFT DOS operating system, power management is generally controlled by the system BIOS (basic input/output system) on the CPU motherboard 12 which monitors activity on the keyboard, mouse and I/O ports to detect situations where the CPU is merely waiting for user input. When the system detects that there has been no user input for a predetermined interval of time, typically around 10 minutes, it executes a power management routine. The power management operations taken by the BIOS may vary depending upon the duration of inactivity. For example, the display 22 may be put in stand-by mode after 10

minutes of inactivity and turned off completely after 45 minutes of inactivity.

Detailed Description Text (4):
One form of power management with regard to the display 22 is the VESA monitor power management protocol. Displays which follow the VESA monitor power management protocol enter different states of power management based on the HSYNC and VSYNC signals output from the video subsystem 14. Table I outlines the VESA monitor power management states.

Detailed Description Text (5):
In addition to enabling display power management responsive to control signals from the system's BIOS, the video subsystem 14 of the present invention also has power management capabilities, such that the power consumed by the video subsystem is greatly reduced with only minimal transition time between reduced-power and normal operation states. Further, the number of operations needed to reduce power are relatively few.

Detailed Description Text (6):
FIG. 2 illustrates a block diagram of the video subsystem 14 of the present invention. In order to more clearly illustrate the power management features, signals which are unnecessary to describe the invention have been condensed or eliminated. Control of the video subsystem is provided by video controller 24. The video controller is coupled to the bus 20 through ADDR lines 26, DATA lines 28 and CONTROL lines 30. The video controller 24 is also coupled to a frame buffer 32 comprising a plurality of VRAM circuits 34 organized in two banks (bank A and bank B ). A VRAM comprises a DRAM whose output is directed to a shift register. The video controller 24 is coupled to the frame buffer 32 via DATA lines 36, ADDR lines 38, SCLK 39 and CONTROL lines 40. The output of the frame buffer 32 is coupled to a RAMDAC 42 which produces the RGB video output to display 22. The RAMDAC 42 is coupled to the video controller 24 via ADDP, lines 44, DATA lines 46, DSCLK 47 and CONTROL lines 48. A phase lock loop circuit 50 (or other clock circuit) outputs a pixel clock (PCLK) 52 to the RAMDAC 42. The PLL 50 also generates a memory clock (MCLK) 54, which is output from the PLL 50 to the video controller 24. The PCLK controls the output of pixels from the RAMDAC 42 to the display 22, while the MCLK controls the video controller 24. DSCLK SCLK are generated from PCLK. DSCLK and SCLK are generally the same frequency. DSCLK can be the same frequency as PCLK or can be divided down.

Detailed Description Text (7):
The video controller 24 controls the PLL 50 using the MODE lines 56, P lines 58 and M lines 59. When used as a card, rather than integrated on the system motherboard, a ROM 60 performs initiation functions not related to power management. The ROM 60 is coupled to the video controller 24 through ADDR lines 62, DATA lines 64 and CONTROL lines 66. The video controller 24 also outputs HSYNC and VSYNC signals to the display 22 on lines 68.

Detailed Description Text (8):
Video controller 24 includes power management circuitry 70 which implements power management procedures to reduce the energy consumed by the video subsystem, and in particular, the display 22, the frame buffer 32, RAMDAC 42, PLL 50 and the video controller 24. Power management in the video subsystem 14 is performed in response to inactivity on the keyboard, mouse and I/O ports. After a certain period of inactivity, the BIOS executes a power management subroutine which, through video controller 24, results in reduced power consumption of the video subsystem 14 and display 22. While the power management circuitry 70 is shown as a block within video controller 24, it should be noted that the circuitry comprises mainly configuration registers 71 (or other memory device) within the video controller 24 which are used by various state machines within the video controller 24 to initiate the signals for reducing power in the video subsystem 14. Exemplary registers and functions are set forth below.

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Detailed Description Text (11):
Disabling PCLK also conserves some power in the video controller 24. Great power savings can be achieved by reducing the frequency of MCLK, since most of the state machines in the video controller 24 will normally be dependent; on MCLK. Since MCLK controls the rate at which the video controller 24 performs the refresh of the DRAM in the VRAMs 34, MCLK must be maintained to preserve the frame buffer data. In the preferred embodiment, MCLK is reduced in frequency to reduce power consumption in the video controller 24, resulting in a corresponding reduction in the refresh rate. In order to refresh the DRAMs properly, the refresh rate, which is set in the video controller 24, is increased to offset the reduction of MCLK frequency.

Detailed Description Text (12):
As described above, the PLL 50 generates both PCLK and MCLK. In the preferred embodiment, the frequency of the PCLK and MCLK signals is programmable in the PLL 50. To reduce the number of lines necessary to program the PLL, both serial and parallel modes are available. In parallel mode, the frequencies of MCLK and PCLK are determined by the values on the M lines 59 and P lines 58, respectively. (In the illustrated embodiment, the M lines 59 are set through jumpers on the video subsystem board.) Since only a limited number of frequencies may be enabled using 4-bit P lines 58 and 3-bit M lines, serial mode uses the P lines 58 to serially transfer data from the video controller 24 to the PLL 50 to program both PCLK and MCLK to frequencies not available, in parallel mode. By turning off PCLK and reducing the frequency of MCLK, the power consumed by the PLL is reduced. The operation of the PLL is described in greater detail in connection with FIG. 3.

Detailed Description Text (21):
In block 86, the display 22 is powered down, for example, by using the VESA power management protocol described above. To place the monitor in the standby state, VSYNC is driven inactive while keeping HSYNC active. A first technique for driving VSYNC inactive is to program the VGA VSYNC Start Register (3D5.10) to a value greater than the VGA Vertical Total Register (3D5.06). The VGA VSYNC Start Register and VGA Vertical Total Register are defined in the VGA specification and must exist for any VGA controller. Alternatively, the video control 24 could contain one or more registers with fields for controlling VSYNC. For example, in the preferred embodiment, a plurality of configuration registers are provided to perform various control functions within the controller 24. By writing a "1" to bit 5 of the Specific Configuration Register 2 (address 3CF.11), the VSYNC is driven inactive. Similarly, to put the monitor into off mode, both HSYNC and VSYNC are driven inactive, This can be performed by writing a "0" into bit 7 of the VGA mode control register (3d5.17). Alternatively, assuming that bit 4 of the Specific Configuration Register 2 control the HSYNC signal, a "1" could be written to bits 4 and 5 to render both VSYNC and HSYNC inactive.

Detailed Description Text (23):
In block 90, the VRAM refresh rate is increased to offset a later reduction in the MCLK frequency. In the illustrated embodiment, the refresh rate of the VRAM is programmably controlled in the video controller 24. Since the operation of the video controller 24 is responsive to the MCLK frequency, the refresh rate is increased by the same factor that the MCLK frequency will be decreased in a later step. Hence,, if the MCLK frequency is to be decreased by a factor of 8, the VRAM refresh rate will be increased by a factor of 8 from the normal rate in order to maintain the normal refresh rate of the VRAM. In the illustrated embodiment, bits 6 and 7 of the Specific Configuration Register 2 control the refresh rate, as shown in Table V.

Detailed Description Text (24):
In the preferred embodiment, the refresh rate is increased by a factor of 8. It should be noted that if the refresh rate is controlled directly through the bus interface, rather than through the video controller 32, it may, or may not, be

necessary to increase the refresh rate at this point. It is necessary to increase the refresh rate only if the later reduction in the MCLK frequency will affect the proper refresh rate of the DRAMs in the VRAM 34.

Detailed Description Text (30):
In block 112, the refresh rate is restored to its normal rate. As shown in Table V, the normal refresh rate is restored by writing "00" to bits 7:6 of the Specific Configuration Register 2.

Detailed Description Text (32):
The present invention provides significant advantages over the prior art. The inactivation of PCLK reduces the power consumed in the RAMDAC 42, frame buffer 32, phase lock loop (PLL) clock circuit 50, and to a smaller extent, the video controller 24. Reducing the frequency of MCLK conserves power in the video controller 24 and the PLL 50, while maintaining the integrity of the data in the frame buffer 32. Significant power savings can be accomplished with minimal BIOS or video controller programming and minimal transfer of state information prior to power-down. It should be noted that power will be conserved in the frame buffer 32 using the preferred embodiment described above, even if DRAMs are used in place of VRAMs in the frame buffer 32.

Detailed Description Paragraph Table (5):
TABLE V Refresh Rate Codes Bit 7 Bit 6 Rate
0 0 Normal 0 1 2*Normal 1 0 4*Normal 1 1 8*Normal

CLAIMS:

1. A method of reducing power consumption in a computer system, comprising the steps of:

generating signals to a display of the computer system to reduce power to the display;

reducing power consumption in a video subsystem of the computer system, comprising the steps of:

inactivating a pixel clock which drives a RAMDAC, thereby reducing power consumed by the RAMDAC; and

decreasing the frequency of a memory clock for driving a video controller by a predetermined factor, thereby reducing the power consumed by the video controller.

2. The method of claim 1 wherein the video controller refreshes a frame buffer at a programmable rate and wherein said step of reducing power consumption in a video subsystem further comprises the step of increasing the programmed refresh rate in the video controller by said predetermined factor, such that the reduction in the memory clock frequency to the video controller is offset by the increase in the programmed refresh rate, resulting in the frame buffer being refreshed at a normal refresh rate.

6. The method of claim 1 wherein said step of decreasing the frequency of a memory clock to the video controller thereby reduces the frequency of memory cycles in a frame buffer, reducing the power consumed by the frame buffer.

7. The method of claim 1 wherein said step of generating signals to a display of a computer system to reduce power to the display comprises the step of generating signals from the video subsystem to enable operation of the display in one of a plurality of monitor power management modes.

11. The computer system of claim 10 wherein the video subsystem further comprises circuitry for increasing the refresh rate of the frame buffer prior to reducing the frequency of said second clock.

16. A method of managing power consumption in a computer system, comprising:

monitoring a computer system for activity;

performing power management in a video subsystem of the computer system in response detecting inactivity in the computer system, comprising the steps of:

increasing the rate at which a video controller refreshes memory in a frame buffer by a predetermined factor; and

decreasing the frequency of a memory clock for driving the video controller by the predetermined factor, thereby reducing the power consumed by the video controller and reducing the frequency of memory cycles to a frame buffer, while maintaining a normal refresh rate.

17. The method of claim 16 wherein the step of performing power management in a video subsystem further comprises the step of inactivating a pixel clock which drives a RAMDAC, thereby reducing power consumed by the RAMDAC.

L3: Entry 29 of 33 File: USPT Jan 28, 1997

DOCUMENT-IDENTIFIER: US 5598565 A
TITLE: Method and apparatus for screen power saving

Abstract Text (1):
A flat panel display power management system for a flat panel display screen in a portable electronic device is disclosed. The flat panel display power management system is capable of controlling the amount of power delivered to each pixel on the flat panel display screen. The portable electronic device can select a subset of important pixels that will continue to receive more power than the remaining pixels if the flat panel display power management system enters a reduced power mode. When the electronic device system determines that the user has been inactive for a predetermined amount of time or if the user manually requests low power mode, the flat panel display power management system enters the reduced power mode. In the reduced power mode, the flat panel display power management system reduces the power provided to the pixels that are not within the subset of important pixels.

Brief Summary Text (2):
The present invention relates to flat panel display systems for portable electronic devices. More specifically, the present invention relates to methods and apparatus for reducing the amount of power consumed by flat panel display system in portable electronic devices.

Brief Summary Text (5):
Some existing portable electronic devices implement power management systems that reduce the amount of power consumed. For example, many portable computer systems contain power management systems that reduce the amount of power consumed by hard disk drive storage devices. The power management system monitors the use of the hard disk drive storage device. If the power management system determines that the hard disk drive has been inactive for a predetermined amount of time, the power management system parks the read/write head of the hard disk drive and spins down the physical hard disk.

Brief Summary Text (6):
Many portable electronic devices use some type of flat panel display system to display information to a user. For example, portable computers, portable televisions, and hand-held video games are constructed using a flat panel display system. Examples of flat panel display systems include active matrix liquid crystal displays, passive matrix liquid crystal displays, electroluminescent displays, field-emission cathode displays, gas-plasma displays, Light Emitting Diode (LED) displays, and Liquid Crystal displays (LCD).

Brief Summary Text (7):
The flat panel display system in a portable electronic device can draw significant amounts of power. It is therefore desirable to implement a power management system that reduces the amount of power consumed by the flat panel display system in a portable electronic device.

Brief Summary Text (9):
It is therefore the object of the present invention to reduce the amount of power used by the flat panel display system of a portable electronic device.

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Brief Summary Text (10):
It is a further object of the present invention to reduce the amount of power used by the flat panel display system while retaining important information on the flat panel display system.

Brief Summary Text (11):
Other objects, features and advantages of the present invention will be apparent from the accompanying drawings, and from the detailed description that follows below. The present invention comprises a flat panel display power management system for a flat panel display system in a portable electronic device. The flat panel display power management system of the present invention is capable of controlling the amount of power delivered to each pixel on the flat panel display screen.

Brief Summary Text (12):
The portable electronic device selects a subset of important pixels that will continue to receive full power if the flat panel display power management system enters a reduced power mode. In the case of a portable computer system, the software running on the portable computer system can select the subset of important pixels.

Brief Summary Text (13):
When the portable electronic system determines that the user has been inactive for a predetermined amount of time, the flat panel display power management system enters the reduced power mode. In the reduced power mode, the flat panel display power management system significantly reduces the amount of power provided to the pixels that are not within the subset of important pixels. The amount of power provided to the pixels in the subset of important pixels may also be reduced for additional power savings.

Brief Summary Text (14):
Alternatively, the user can manually request the portable electronic system to enter the reduced power mode. For example, if a user only needs to view a small portion of the flat panel display system, the user may request the portable electronic system to provide full power to the pixels within that small portion of the flat panel display system.

Drawing Description Text (4):
FIG. 2 illustrates a portable computer system with a flat panel display power management system for controlling the amount of power consumed by the flat panel display system;

Drawing Description Text (5):
FIG. 3a illustrates a screen display of drawing program running on a portable computer system;

Drawing Description Text (6):
FIG. 3b illustrates the screen display of a portable computer system of FIG. 3a when the flat panel display power management system is activated and the cursor is on the pull-down menu;

Drawing Description Text (7):
FIG. 3c illustrates the screen display of a portable computer system of FIG. 3a when the flat panel display power management system is activated and all pixels on the flat panel display receive reduced power;

Drawing Description Text (8):
FIG. 3d illustrates the screen display of a portable computer system of FIG. 3a when the flat panel display power management system is activated and the cursor is on the toolbar;

Drawing Description Text (9):
FIG. 3e illustrates the screen display of a portable computer system of FIG. 3a when the flat panel display power management system is activated and the cursor is in the main drawing area;

Drawing Description Text (10):
FIG. 3f illustrates an alternate embodiment of the screen display of FIG. 3e when the flat panel display power management system is activated and the cursor is in the main drawing area;

Drawing Description Text (11):
FIG. 4a illustrates the screen display of a portable computer system running a word processing program when the flat panel display power management system is activated and an I-beam cursor is in the text area;

Drawing Description Text (12):
FIG. 4b illustrates the screen display of a portable computer system running a word processing program that does not configure the flat panel display power management system;

Drawing Description Text (13):
FIG. 4c illustrates the screen display of a portable computer system configured in a manner that allows more than one area on the display to be designated as the important area;

Drawing Description Text (14):
FIG. 5 illustrates a single frame of a screen display of a portable television or animated computer display configured in a manner that illuminates the pixels in a foreground image and reduces power to the pixels of the background images.

Detailed Description Text (2):
The present invention discloses methods and apparatus for reducing the amount of power drawn by a flat panel display system. In the following description, for purposes of explanation, specific nomenclature is set forth to provide a thorough understanding of the present invention. Furthermore, well known circuits and devices are shown in block diagram form in order not to obscure the present invention unnecessarily. Moreover, it will be apparent to one skilled in the art that these specific details are not required in order to practice the present invention.

Detailed Description Text (3):
The present invention is disclosed in the context of a portable computer device that incorporates a flat panel display system for displaying information. However, it will be appreciated by those skilled in the art that the teachings of the present invention can be incorporated into any electronic device that incorporates a flat panel display system.

Detailed Description Text (6):
The Input/Output (I/O) Bridge 130 of portable computer device 100 drives several input and output devices coupled to an I/O bus 135. For example, the portable computer device 100 illustrated in FIG. 1 comprises cursor control device 140 and keyboard 150 as input devices; hard disk drive 160 and floppy disk drive 165 as storage devices (input and output); and display driver 170 driving an output display 180 as an output device.

Detailed Description Text (10):
The output display 180 of most portable computer devices comprises a flat panel display system. The flat panel display system can draw significant amounts of power from the battery used to power the portable computer device 100. It is therefore

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desirable to implement a method of reducing the power consumed by the flat panel display system of the portable computer device 100.

Detailed Description Text (12):
Several flat panel display systems operate by providing power to each individual pixel creating the image on the flat panel display that is to be displayed. The power provided to each pixel in such systems causes the pixel to emit a point of light. Examples of light emissive flat panel display systems include electroluminescent displays, field-emission cathode displays, color gas-plasma displays, and Light Emitting Diode (LED) displays.

Detailed Description Text (13):
To reduce the amount of power consumed by a light emissive flat panel display system, the present invention introduces a flat panel display power management system that is capable of controlling the amount of power provided to each individual pixel on the display. FIG. 2 illustrates the portable computer device 100 of FIG. 2 with the added flat panel display power management system 195. To conserve power in a portable computer device that uses a light emissive flat panel display system, the flat panel display power management system 195 reduces the amount of power provided to certain pixels on the flat panel display screen.

Detailed Description Text (14):
Other flat panel display systems operate by overlaying a matrix of pixels on top of a backlight. Such flat panel display systems generate an image by selectively allowing the backlight through the matrix of pixels. Examples of flat panel display systems that operate using a backlight include active matrix Liquid Crystal Displays (AMLCD) and passive matrix Liquid Crystal Displays (LCD).

Detailed Description Text (15):
To reduce the amount of power consumed by a flat panel display system that operates using a backlight, the flat panel display power management system 195 of the present invention can be configured to reduce the refresh rate of the flat panel display system. For example, the flat panel display power management system 195 may reduce the frame rate such that the display is updated half as often as normal. Alternatively, the flat panel display power management system 195 may reduce the frame updates to pixels in unimportant areas. Although, this specification will focus on reducing the power consumed by light emissive flat panel display systems, the teachings are also applicable to backlighted flat panel displays.

Detailed Description Text (16):
The flat panel display power management system of the present invention can be invoked by the operating system of the portable computer device 100. The operating system monitors the input devices utilized by a user. For example, in the portable computer device 100 illustrated in FIG. 2, the operating system of the portable computer device 100 monitors the keyboard 150 and cursor control 140 input devices. If the input devices have been inactive for a predetermined time limit, the operating system instructs the flat panel display power management system 195 of the present invention to enter its power conservation mode.

Detailed Description Text (17):
Alternatively, the flat panel display power management system 195 can be configured such that a user can manually control when the power conservation mode is entered. Providing control to the user allows the user to reduce the power consumed by the flat panel display in situations where the user is willing to trade reduced visibility of the screen for additional operating time while operating off of a battery.

Detailed Description Text (18):
The flat panel display power management system 195 of the present invention is context sensitive such that the flat panel display power management system 195

attempts to reduce screen power in a manner that is least offensive to the user. Specifically, the flat panel display power management system 195 of the present invention attempts to reduce the power provided to pixels that are the least important to the user while providing more power to the pixels in the area of the screen where the user's attention is focused.

Detailed Description Text (19):
The flat panel display power management system 195 of the present invention allows each individual software program to determine which pixels are important to the user and which pixels are not as important. Each software program can continually adjust the settings of the flat panel display power management system 195 such that different pixels are considered important at different times. An example of this effect is provided with reference to FIGS. 3a, 3b, 3c, 3d, 3e and 3f.

Detailed Description Text (21):
The drawing program selects the important pixels based upon where the cursor 340 is placed on the display screen. When the flat panel display power management system 195 is enabled by the user or the operating system, the flat panel display power management system 195 provides reduced power to the pixels not in the selected set of important pixels. The selected important pixels may received full power such that the selected important pixels will easily be visible. Alternatively, the selected important pixels may also receive less power than in a normal operating mode such that additional power savings are achieved.

Detailed Description Text (22):
FIG. 3b illustrates how the display screen appears when the user or the operating system activates the flat panel display power management system 195 and the cursor 340 is on the pull-down menu 310. As illustrated in FIG. 3b, the pixels that comprise pull-down menu 310 receive more power than the other pixels such that the pull-down menu 310 remains clearly visible to the user. The remainder of the pixels receive significantly reduced power such that the amount of power consumed by the display screen is drastically reduced.

Detailed Description Text (23):
FIG. 3c illustrates an alternate embodiment of how the display screen may appear if the user or the software activates the flat panel display power management system 195 and the cursor 340 is on the pull-down menu 310. As illustrated in FIG. 3c, the pixels that comprise pull-down menu 310 receive more power than the other pixels. However, the power provided to the pixels comprising the pull-down menu 310 is not full power such that even the pixels important area receive reduced power. Again, the remainder of the pixels on the display screen receive significantly reduced power such that the amount of power consumed by the display screen is reduced.

Detailed Description Text (24):
FIG. 3d illustrates how the display screen appears when the user or the software enables the flat panel display power management system 195 and the cursor 340 is on the drawing toolbar 330. As illustrated in FIG. 3d, the pixels that comprise drawing toolbar 330 receive more power than the other pixels such that the drawing toolbar 330 remains visible to the user. Thus, the drawing program adjusts the subset of pixels considered to be important based upon the position of the cursor 340.

Detailed Description Text (25):
FIG. 3e illustrates how the display screen may appear if the user or the software enables the flat panel display power management system 195, and the cursor 340 is in the main drawing area 320. As illustrated in FIG. 3e, a rectangle of pixels in the main drawing area 320 that surround the cursor receive more power than the other pixels such that the area where the user is working remains visible to the user.

Detailed Description Text (26):
FIG. 3f illustrates an alternate embodiment of how the display screen may appear if the user or the operating system enables the flat panel display power management system 195 and the cursor 340 is in the main drawing area 320. As illustrated in FIG. 3f, a circle of pixels surrounding the cursor 340 in the main drawing area 320 receive more power than the other pixels on the display. In a drawing program, a circle of pixels surrounding the cursor 340 may provide a better focus area.

Detailed Description Text (27):
As stated above, each individual software program can configure how the flat panel display power management system 195 will reduce power to the flat panel display system. FIGS. 4a, 4b, and 4c illustrate a second example of how a program can select the pixels that will be receive reduced power.

Detailed Description Text (28):
FIG. 4a illustrates how a word processing program appears after the flat panel display power management system 195 has been activated manually by the user of the system using screen power save checkbox 420. The word processing program uses an "I-beam" cursor 410 to indicate where any text typed by the user will appear next. As illustrated in FIG. 4a, the word processing program causes the flat panel display power management system 195 to provide greater power to the pixels of two adjacent lines of text wherein the second line of text is the line of text containing the I-beam cursor 410. The remaining pixels receive significantly reduced power. The configuration illustrated in FIG. 4a is ideal for a situation where the user only plans to input information and thus is not concerned with be able to see the surrounding text. For example, if the user is in a meeting taking notes for future use, the user can manually enter the reduced power mode such that the battery lifetime will be extended.

Detailed Description Text (29):
Not all software programs will configure the flat panel display power management system 195 with a set of pixels that should receive more power than the remaining pixels. If the flat panel display power management system 195 is not configured with a set of important pixels that should receive more power than the remaining pixels in a reduced power state, the flat panel display power management system 195 can enter a default reduced power state. In the default reduced power state, the flat panel display power management system 195 simply provides more power to the pixels comprising a rectangle surrounding the cursor.

Detailed Description Text (30):
FIG. 4b illustrates how the word processing program of FIG. 4a can appear if the word processing program does not configure the flat panel display power management system 195. As illustrated in FIG. 4b, the default reduced power state causes the flat panel display power management system 195 to provide full power to the pixels that define a rectangle surrounding the I-beam cursor 410.

Detailed Description Text (31):
The user may not always concentrate on a single focus area. For example, when there is more than one cursor on the display, the user may focus his attention on both cursor positions. In order to accommodate such situations, the flat panel display power management system 195 of the present invention can be constructed in a manner that allows more than one area on the display to be designated as the important area. FIG. 4c illustrates an example of this situation.

Detailed Description Text (32):
Referring to FIG. 4c, a word processing program is running in a window on the flat panel display. Within the word processing program window is I-beam cursor 410. Also on the display is pointer cursor 340. FIG. 4c illustrates how both the text around I-beam cursor 410 and the pulldown menu bar under pointer cursor 340 received more power than the rest of the display.

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Detailed Description Text (33):
If the flat panel display power management system 195 remains in the low power state for an extended period of time, the flat panel display power management system 195 can enter an extra low power mode. In the extra low power mode, the flat panel display power management system 195 turns off all the pixels on the flat panel display system. To remind the user that the portable computer device is still on, the flat panel display power management system 195 occasionally flashes the important pixels selected for the normal reduced power mode.

Detailed Description Text (35):
Flat panel display systems are increasingly being used to display dynamic images. For example, portable television systems, hand-held video games, and computer systems utilizing animation all display dynamic images.

Detailed Description Text (36):
The present invention can be used to reduce the power used by a flat panel display system that is displaying a dynamic image. To reduce the power used by a flat panel display system displaying dynamic images, the flat panel display power management system 195 reduces the pixels updates to unimportant areas. As explained earlier, this technique can also be applied to flat panel display systems that rely on backlighting, such as passive matrix flat panel display systems and active matrix flat panel display systems. An example of this technique is provided with reference to FIG. 5.

Detailed Description Text (37):
Referring to FIG. 5, a single frame of a screen display of a portable television or animated computer display in which important foreground information is displayed full power and less important background information receives less power. As illustrated in FIG. 5, the pig 510 moving around in the foreground is displayed with full power. The remaining pixels comprising the background are not refreshed as often since those pixels are associated with a static background. The pixels receiving full power change on a frame-by-frame basis depending upon important information for that frame.

Detailed Description Text (38):
In the foregoing specification, the invention has been described with reference to the specific embodiment of a portable computer system. However, it will be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the following claims. Thus, it will be appreciated by those skilled in the art that the teachings of the present invention can be incorporated into any electronic device that incorporates a flat panel display system. For example, the teachings of the present invention can be applied towards portable televisions and hand-held video games that are constructed using a flat panel display system. Accordingly, the specification and drawings are to be regarded in an illustrative sense rather than a restrictive sense.

CLAIMS:

1. An apparatus for conserving power in a portable electronic device, said apparatus comprising:

a flat panel display system, said flat panel display system providing an output display for said portable electronic device, said flat panel display system comprising a plurality of individual pixels;

a flat panel display power management system, said flat panel display power management system coupled to said flat panel display system, said flat panel display power management system providing a controllable amount of power to each of

said plurality of individual pixels such that each of said plurality of individual pixels may be displayed at a different level of visibility;

a processor in said electronic device; and

a software program running on said processor in said portable electronic device, said software program configuring said flat panel display power management system such that said software program determines a subset of said plurality of pixels that will receive more power than pixels not in said subset if said flat panel display power management system enters an active state.

2. An apparatus for conserving power in a portable electronic device, said apparatus comprising:

a flat panel display system, said flat panel display system providing an output display for said portable electronic device, said flat panel display system comprising a plurality of individual pixels;

a cursor displayed on said flat panel display system; and

a flat panel display power management system, said flat panel display power management system:

coupled to said flat panel display system;

providing a controllable amount of power to each of said plurality of individual pixels such that each of said plurality Of individual pixels may be displayed at a different level of visibility; and

having a default reduced power mode, said default reduced power mode providing more power to a subset of pixels defining a shape around said cursor than to pixels not within said subset.

3. An apparatus for conserving power in a portable electronic device, said apparatus comprising:

a flat panel display system, said flat panel display system providing an output display for said portable electronic device, said flat panel display system comprising a plurality of individual pixels; and

a flat panel display power management system, said flat panel display power management system:

coupled to said flat panel display system;

providing a controllable amount of power to each of said plurality of individual pixels such that each of said plurality of individual pixels may be displayed at a different level of visibility; and

having an extra low power mode, said extra low power mode turning off all of said plurality of pixels and periodically flashing said subset of pixels.

4. The apparatus for conserving power in a portable electronic device as claimed in claim 1 wherein said flat panel display system comprises an electroluminescent display system.

5. The apparatus for conserving power in a portable electronic device as claimed in claim 1 wherein said flat panel display system comprises a field-emission cathode display system.

6. The apparatus for conserving power in a portable electronic device as claimed in claim 1 wherein said flat panel display system comprises a gas-plasma display system.

7. The apparatus for conserving power in a portable electronic device as claimed in claim 1 wherein said flat panel display system comprises a Light Emitting Diode (LED) display system.

8. A method for conserving power in a portable electronic device, said method comprising the steps of:

selecting a subset of important pixels from a flat panel display system that comprises a plurality of pixels;

configuring a flat panel display power management system in said portable electronic device by providing said subset of important pixels to said flat panel display power management system; and

entering a reduce power mode wherein said flat panel display power management system provides more power to said subset of important pixels than to pixels not within said subset.

9. The method for conserving power in a portable electronic device as claimed in claim 8 wherein said steps of selecting a subset of important pixels and configuring a flat panel display power management system are performed by a software program running on said portable electronic device.

10. The method for conserving power in a portable electronic device as claimed in claim 8 wherein said steps of selecting a subset of important pixels and configuring a flat panel display power management system are not performed then said flat panel display power management system enters a default reduced power mode, said default reduced power mode providing more power to a subset of pixels defining a shape around a cursor on said flat panel display than to pixels not in said subset of pixels defining a shape around said cursor.

11. The method for conserving power in a portable electronic device as claimed in claim 8 wherein said flat panel display power management system further comprises an extra low power mode, said extra low power mode turning off all of said plurality of pixels and periodically flashing said subset of important pixels.

12. The method for conserving power in a portable electronic device as claimed in claim 9 wherein said flat panel display system comprises an electroluminescent display system.

13. The method for conserving power in a portable electronic device as claimed in claim 9 wherein said flat panel display system comprises a field-emission cathode display system.

14. The method for conserving power in a portable electronic device as claimed in claim 9 wherein said flat panel display system comprises a gas-plasma display system.

15. The method for conserving power in a portable electronic device as claimed in claim 9 wherein said flat panel display system comprises a Light Emitting Diode (LED) display system.

16. An apparatus for conserving power in a portable electronic device, said apparatus comprising the elements of:

a flat panel display system, said flat panel display system providing an output

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display for said portable electronic device, said flat panel display system comprising a plurality of individual pixels; and

a flat panel display power management system, said flat panel display power management system coupled to said flat panel display system, said flat panel display power management system providing a controllable amount of power to each of said plurality of individual pixels such that each of said plurality of individual pixels may be displayed at a different level of visibility, said flat panel display power management system also for reducing the rate at which each of said plurality of individual pixels changes display states, allowing each of said plurality of individual pixels to be refreshed at different times.

17. The apparatus for conserving power in a portable electronic device as claimed in claim 16 wherein said flat panel display system comprises an active matrix liquid crystal display system.

18. The apparatus for conserving power in a portable electronic device as claimed in claim 16 wherein said flat panel display system comprises a passive matrix liquid crystal display system.

L3: Entry 31 of 33 File: USPT Nov 15, 1994

DOCUMENT-IDENTIFIER: US 5365487 A
TITLE: DRAM power management with self-refresh

Brief Summary Text (9):
One way to reduce the required electrical power occurs by placing the personal computer in a so called sleep mode by active, idle or automatic entry. In this mode, the personal computer maintains the data in the DRAMs and maintains electrical power to the DRAMs. Refresh occurs by the DRAMs entering an internal, self-refresh mode with refresh occurring at a slower rate, which reduces the power used by the DRAMs This saves the electrical power needed to operate the disk drives, but costs the power needed to maintain the data in the DRAMs for possibly extended periods.

Brief Summary Text (16):
The present invention achieves reduced power consumption in DRAM parts during a sleep mode effected in the associated computer system through the use of power management circuits. These power management circuits reduce the power in first circuits needed for the DRAM parts to effect an internal or self-refresh of the contained data and reduce or eliminate the power consumed by other or second circuits in the DRAM parts during self-refresh.

Detailed Description Text (2):
In FIG. 1, computer system 20 furnishes central processing unit 22, keyboard control 24, display control 26, power supply 28, dynamic random access memory (DRAM) 30, disk drive 32 and ROM 34. These different parts connect together through data bus 36, address bus 38 and control bus 40. Keyboard control 24 connects to keyboard 42 over leads 44 and display control 26 connects to display 46 over leads 48. Power supply 28 includes provisions for battery 50 and can connect to line power through plug 52.

Detailed Description Text (24):
The self-refresh occurs at a rate reduced from a normal refresh rate by the power management circuits reducing the frequency of an internal oscillator. The power management circuits also operate first circuits, which are required to operate to effect the self-refresh, substantially only at the refresh of a row of memory cells. The power management circuits also remove normally applied electrical power from second circuits in the dynamic random access memory parts; the second circuits do not need to operate and can have power removed during the refresh of row of memory cells.

CLAIMS:

16. The computer system of claim 1, wherein the computer system includes keyboard control circuits, display control circuits, disk drive circuits and ROM circuits connected to the central processing unit and memory circuits.

31. A process of maintaining data in a personal computer, the process comprising:

receiving a user indication of a sleep mode;

retaining data in dynamic random access memory pans in the personal computer during the sleep mode;

producing signals to the dynamic random access memory parts indicating the sleep mode is to be effected;

effecting, in response to the producing signals to the dynamic random access memory parts indicating the sleep mode is to be effected, self-refresh of dynamic memory cells in the dynamic random access memory pans, the effecting including reducing the self-refresh rate from a normal refresh rate and operating first circuits that are required to operate to effect the self-refresh substantially only at refresh of a row of memory cells; and

removing, in response to the producing signals to the dynamic random access memory parts indicating the sleep mode is to be effected, electrical power that is normally applied to second circuits included in the dynamic random access memory parts that can have power removed during the self-refresh.

32. The process of claim 31, wherein the reducing the self-refresh rate includes reducing the frequency of an oscillator in the memory part.